REMARKS

Applicant has amended the specification on page 3 deleting the reference numeral 8 and substituting the reference numeral 7 as suggested by the Examiner. Applicant has also amended page 8, line 19, to correct the reference numeral "103" to read –132--. In addition, applicant has amended page 10 of the specification to substitute the word "vias" for the word "channel" to conform the specification to the original wording of claim 1. In addition, a replacement sheet for Figure 1 has been attached for review and approval by the Examiner. In the replacement sheet of Figure 1, the reference numeral 19 is now included in Figure 1 consistent with the description on page 10 and includes both the metal conductive layer 18 and the conductive paste material 180. In making the above amendments, no new matter has been entered into the application.

The rejection of claims 1-12 under 35 USC 112, first paragraph, as failing to comply with the written description is respectfully traversed. The "plurality of conductive through vias" as recited in the original version of claim 1 clearly corresponds to the channel 19 in the second paragraph of page 10 of the specification. Accordingly, to conform the claims to the specification the word "vias" is substituted for the word "channel". Figure 1 has also been revised so that it is clear that the vias 19 as indicated on page 10 comprise a metal conductive layer 18 with the rest of the cavity filled with the conductive paste 180. Stated otherwise, the conductive vias 19 represent the layer 18 and the filler compound 180. Claims 1 and 7 are now consistent with the specification and the rejection of claims 1-12 under the first paragraph of 35 USC 112 should be withdrawn.

Claims 1 and 7 have also been amended to overcome the rejection of claims 1-12 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 7 have been extensively amended to clarify the claims to remove all ambiguity and indefiniteness from the claims. The amendment to claim 7 also provides clear antecedent basis for claim 12. Accordingly, the rejection of claims 1-12 under 35 USC 112, second paragraph, should also be withdrawn.

IN THE DRAWINGS:

Attached hereto is a replacement sheet for Figures 1 and 3 for review and approval by the Examiner. Figure 1 has been modified to include the reference numeral 19.

The rejection of claims 1-12 under 35 USC 103(a) as being unpatentable over Asada (U.S. Patent 6,239,496) in view of Heo (U.S. Patent 6,555,917) and applicants admitted prior art (AAPA) is respectfully traversed.

Applicant's invention is directed to a stacked flip-chip package comprising two chip carriers, each of which includes at least a chip and a plurality of solder bumps formed on the active surface of the chip to electrically connect the chip to the chip carrier. A first chip carrier is joined with a second chip carrier via an insulating adhesive applied on the inactive surface of the first chip mounted on the first chip carrier. The insulating adhesive is also applied to the inactive surface of the second chip mounted on the second chip carrier, such that the two inactive surfaces are bonded together to form a multichip module. As both the topmost and lowermost surfaces of the multichip module are electrically connected with other components, vertical stacking techniques may be adopted in the flip-chip structure, to result in a more flexible chip arrangement in the multichip semiconductor package.

Claims 1 and 7 have been amended in conjunction with the above explanation so that it is clear that the first chip carrier is mounted with at least a first chip having a first active surface and a first non-active surface opposite to the first active surface, a corresponding second chip carrier having a second active surface and a second non-active surface opposite to the second active surface, an adhesive layer for attaching the first non-active surface of the first chip to the second non-active surface of the second chip, a resin encapsulating layer filled in between the first chip carrier and the second chip carrier and a plurality of conductive vias penetrating the first chip carrier, the resin encapsulating layer and the second chip carrier so that the second chip carrier is electrically connected to the first chip carrier via the conductive vias. In claims 1 and 7 solder bumps are formed on the first active surface of the first chip carrier for connecting the first chip to the first chip carrier and solder bumps are formed on the second active surface of the second chip for connecting the second chip to the second chip carrier. In claim 1 as amended, the plurality of conductive vias penetrate the first chip carrier, the resin encapsulating layer and the second chip carrier whereas in amended claim 7 the

plurality of conductive traces are formed over the first chip carrier, the resin encapsulating layer and the second chip carrier.

Asada discloses a multichip module assembled by the package having very thin semiconductor chip. However, the flip-chip semiconductor package in Asada provides no teaching or suggestion to employ solder bumps for connecting the chips to the corresponding chip carriers nor does Asada teach the use of a plurality of conductive vias for penetrating the first and second chip carriers as claimed in claim 1 or teach the use of a plurality of conductive traces formed over the first and second chip carriers and the resin encapsulating layer for electrically connecting the first and second chip carriers as taught and claimed in claim 7.

Instead, the solder balls (641a, ..., 641j or 651a,.....654a) in Asada are either used for connecting the chip to the wiring layer or for connecting one connection land to another. Therefore, the solder balls in Asada are not the equivalent of solder bumps for connecting the chips to the corresponding chip carriers. Moreover the alleged conductive through vias 251-253 in Asada are merely stud conductors buried in the through holes in the insulating substrate. They are not intended as conductive vias for penetrating the first and second chip carriers and the resin encapsulating layer. Moreover, Asada's wiring layer 121-124 and inner leads 721-723 also do not teach or suggest applicant's conductive traces over the first and second chip carriers and the resin encapsulating layer for electrically connecting the first and second chip carriers.

Although Heo teaches an adhesive layer there is no teaching or suggestion of using a plurality of conductive vias penetrating the first chip carrier, the resin encapsulating layer, and the second chip carrier as recited in claim 1, or for using conductive traces formed over the first chip carrier, the resin encapsulating layer, and the second chip carrier as recited in claim 7. As a result, applicants flip-chip semiconductor package is a completely different arrangement from that taught in Asada taken alone or in combination with Heo.

For the foregoing reasons, claims 1 and 7 are believed to be patentable over Asada in view of Heo and AAPA. Claims 2-6 and 8-12 are dependent claims which are believed patentable for at least the same reasons as given above.

New claims 13-18 have been added as dependent claims depending from claims 1 and 7. The new claims relate to the conductive vias and other elements for encapsulating the conductive traces which are not taught or suggested in the cited references.

Reconsideration and allowance of claims 1-18 is respectfully solicited.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450 on October 5, 2004.

Date: Oct. 5, 2004

Amended Section of Page 3 of Specification:

As shown in ~~FIG. 8~~ FIG. 7, this multichip module comprises two conductive layers, a first chip conductive layer 50 and a second conductive layer 53, which are respectively connected to a first chip 51 and a second chip 54 in a flip-chip manner.

Amended Section of Page 8 of Specification:

.....second chip 14 to be transmitted to the ball pads mounted on the non-active surface 101, 131 of the chip carrier 10, 13 through the conductive traces (not shown) which extend axially through the vias 102, ~~103~~ 132.

Amended Section of Page 10 of Specification:

.....the bottom of the first chip 11 and the ~~second d chip~~ second chip 14 to be completely filled with the resin encapsulating materials. As R-MASK resin has lower hyproscopicity and viscosity compared to the conventional resin, it is unlikely for the formed resin encapsulating layer 17 to absorb too much moisture which can result in popcorn. This resin encapsulating material is also advantageous in that it can completely fill in the gaps between the adjacent solder bumps, and therefore an additional refilling process is not required, simplifying the manufacturing process.

After the resin encapsulating layer 17 is formed, a so-called hole formation technique is applied to form ~~a conductive channel~~ conductive vias 19 that ~~interconnects~~ interconnect the through hole 102 of the first chip carrier 10 and the through hole 132 of the second chip carrier 13. The conductive ~~channel~~ vias 19 further comprises a metal conductive layer 18 made of copper foil on the inner wall of the conductive channel, and the rest of the cavity is then filled with conductive materials 180 such as copper paste or silver paste or dielectric materials such as epoxy resin. This conductive ~~channel~~ vias 19 ~~allows~~ allow the second chip carrier 13 to be electrically connected to the first chip carrier 10.

What is claimed is:

1. (Currently Amended) A flip-chip semiconductor package, comprising:

a first chip carrier ~~accommodating~~ mounted with at least ~~one~~ a first chip having ~~an~~ a first active surface and a first non-active surface opposite to the first active surface wherein ~~on which~~ a plurality of first solder bumps are formed on the first active surface for electrically connecting the first chip to the first chip carrier~~, and an opposing non-active surface~~;

a second chip carrier ~~accommodating~~ mounted with at least ~~one~~ a second chip having ~~an~~ a second active surface ~~on which~~ and a second non-active surface opposite to the second active surface wherein a plurality of second solder bumps are formed on the second active surface for electrically connecting the second chip to the second chip carrier~~, and an opposing non-active surface~~;

an adhesive layer, applied over the first non-active surface of the ~~fist~~ first chip for attaching the first non-active surface of the first chip to ~~allowing~~ the second non-active surface of the second chip ~~of the second chip carrier to be attached to the first chip of the first chip carrier~~;

a resin encapsulating ~~layer,~~ layer filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the ~~plurality of~~ first and second solder bumps; and

a plurality of conductive ~~through~~ vias ~~extending axially between~~ penetrating the first chip carrier, the resin encapsulating layer, and the second chip carrier ~~for electrically connecting~~ so that the ~~first~~ second chip carrier is electrically connected to the first chip carrier via ~~the second chip carrier and~~ the conductive ~~through~~ vias.

2. (Original) The flip-chip semiconductor package of claim 1, wherein a plurality of solder bumps are disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

3.(Original) The flip-chip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a substrate.

4.(Original) The flip-chip semiconductor package of claim 1, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).

5. (Original) The flip-chip semiconductor package of claim 1, wherein the adhesive layer is an insulating adhesive having high elasticity.

6. (Original) The flip-chip semiconductor package of claim 1, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.

7. (Currently Amended) A flip-chip semiconductor package, comprising:

a first chip carrier ~~accommodating~~ mounted with at least ~~one~~ a first chip having ~~an~~ a first active surface and a first non-active surface opposite to the first active surface, wherein ~~on which~~ a plurality of first solder bumps are formed on the first active surface for electrically connecting the first chip to first chip carrier~~, and an opposing non-active surface~~;

a second chip carrier ~~accommodating~~ mounted with at least ~~one~~ a second chip having ~~an~~ a second active surface and a second non-active surface opposite to the second active surface, wherein ~~on which~~ a plurality of second solder bumps are formed on the second active surface for electrically connecting the second chip to second chip carrier~~, and an opposing non-active surface~~;

an adhesive layer, applied over the first non-active surface of the ~~fist~~ chip for attaching the first non-active surface of the first chip to ~~allowing~~ the second non-active surface of the second chip ~~of the second chip carrier to be attached to the first chip of the first chip carrier~~;

a resin encapsulating ~~layer,~~ layer filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the ~~plurality of~~ first and second solder bumps; and

a plurality of conductive traces formed ~~between~~ over the first chip carrier, the resin encapsulating layer, and the second chip carrier ~~for electrically connecting~~ such that the ~~first~~ second chip carrier is electrically connected to the first chip carrier via ~~each of~~ the conductive traces.

8. (Original) The flip-chip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a substrate.

9. (Original) The flip-chip semiconductor package of claim 7, wherein each of the first chip carrier and the second chip carrier is a tape carrier (TAB).

10. (Original) The flip-chip semiconductor package of claim 7, wherein the adhesive layer is an insulating adhesive having high elasticity.

11. (Original) The flip-chip semiconductor package of claim 7, wherein the resin encapsulating layer is made of resin materials having low hygrosocopicity and low viscosity.

12. (Currently Amended) The flip-chip semiconductor package of claim 7, wherein each of the conductive traces ~~have~~ has one end connected to ~~the~~ a second bond pad ~~ball pads~~ of the second chip carrier and the other end connected to ~~the ball pads~~ a first bond pad of the first chip carrier.

13. (New) The flip-chip semiconductor package of claim 1, wherein the conductive vias include a plurality of through holes opening through the first chip carrier, the resin encapsulating layer, and the second chip carrier.

14. (New) The flip-chip semiconductor package of claim 13, wherein a conductive layer is formed on an inner wall of each of the through holes to define a cavity.

15. (New) The flip-chip semiconductor package of claim 14, wherein the conductive layer is made of a copper foil.

16. (New) The flip-chip semiconductor package of claim 14, wherein the cavity is filled by a conductive material.

17. (New) The flip-chip semiconductor package of claim 14, wherein the cavity is filled by a dielectric material.

18. (New) The flip-chip semiconductor package of claim 7, further comprising a dielectric solder mask for encapsulating the conductive traces.